UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/743,929	01/16/2001	Silvia Gohlke	P- 00,1958	8930

7590 05/12/2004

MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 300
MCLEAN, VA 22102

EXAMINER	
GOFF II, JOHN L	
ART UNIT	**PAPER NUMBER**
1733	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/743,929	GOHLKE ET AL.	
	Examiner	Art Unit	
	John L. Goff	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment received 2/25/04. The previous claim objections have been overcome.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 10-16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa (JP 06097656 A, Abstract of JP 06097656 A, and Machine translation of JP 06097656 A) in view of Sato et al. (U.S. Patent 4,882,455), Polinski (U.S. Patent 5,708,570), and Lin et al. (U.S. Patent 5,242,867).

Nishikawa is directed to a method for producing a ceramic multilayer board (substrate for carrying semiconductors, etc. which is capable of being used in a high frequency module) wherein the board comprises at least one planar electrode connected to electrical

interconnections, at least one layer composed of a first green sheet, which becomes compacted in a first temperature interval, and at least one layer composed of a second green sheet, which becomes compacted at a second temperature interval that is different from the first temperature interval (See Figures 1-3, the abstract lines 1-9, and the translation page 2, paragraph 11). Nishikawa teaches compacting the first green sheet at the temperature interval between 600 and 1000 °C and compacting the second green sheet at the temperature interval between 800 and 1500 °C. Nishikawa further teaches forming the planar electrodes and electrical interconnections from a conductive metal paste comprising metals such as copper, palladium, platinum, and/or silver (See the translation page 3, paragraphs 21 and 23). Nishikawa is silent as to forming the electrodes from a metal foil as opposed to the conductive metal paste. It would have been well within the purview of one of ordinary skill in the art at the time the invention was made to form the electrodes taught by Nishikawa from metal foil as it was well known in the art, e.g. the art of forming ceramic circuit boards, to form electrodes from metal foils, conductive metal pastes, and combinations thereof as shown for example by Sato et al. and only the expected results would be achieved.

It is further noted Nishikawa as modified by Sato et al. are silent as to a specific teaching of the first and second green sheets having substantially identical coefficients of expansion (of for example between 6 and 7 ppm/K). However, one of ordinary skill in the art at the time the invention was made would have readily appreciated using in Nishikawa as modified by Sato et al. green layers having substantially identical coefficients of expansion as was well known in the art and shown for example by Polinski to ensure the layer stack does not crack and/or distort after compacting. Furthermore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to use first and second green sheets in Nishikawa as modified by Sato et al. and Polinski having thermal coefficients of expansion below 8 ppm/K such that the coefficients of expansion of the green layers essentially match those of the additional layers within the multilayer, e.g. electrodes, metal foils, conductive paste, etc., thus preventing the additional layers from cracking or distorting as was well known in the art as shown for example by Lin et al.

Regarding claim 11, Nishikawa teaches a number of different layer stack sequences having different properties/functions (See Figures 1-3). One of ordinary skill in the art at the time the invention was made would have readily appreciated that Nishikawa does not show all possible layer stack combinations and it would not have required undue experimentation to form alternative layer stack combinations having different properties/functions. Furthermore, it is noted Nishikawa teaches two sequences wherein a layer stack having a layer sequence in one direction is arranged on top of a layer stack having the same sequence in an opposite direction (Figures 1 and 2).

Sato et al. are directed to electronic circuit substrates. Sato et al. teach forming conductor circuits on the electronic circuit substrates using conventional techniques including adhering a metal foil, applying a conductive paste, and combinations thereof (Column 5, lines 21-29).

Polinski is directed to a ceramic structure comprising electronic components, a plurality of green layers, and shrinkage control layers (Figure 2 and Column 4, lines 28-32 and 43-45). Polinski teaches that the coefficients of expansion for the electronic components, green layers, and shrinkage control layers substantially match to ensure the structure does not crack and/or distort after firing (Column 1, lines 50-57 and Column 4, lines 17-23 and 45-48).

Lin et al. disclose ceramic multilayer substrates for use in manufacturing electronic packages. Lin et al. teach the ceramic layers have expansion coefficients of 3-8 ppm/°C such that the coefficients of the ceramic layers essentially match those of the additional layers within the multilayer thus preventing the additional layers from cracking (Column 1, lines 26-29 and Column 3, lines 6-19 and Column 6, lines 62-68 and Column 7, lines 1-6).

Response to Arguments

5. Applicant's arguments filed 2/25/04 have been fully considered but they are not persuasive.

Applicant argues, "Nishikawa describes a ceramic multilayer body with ceramic layers made of different ceramic materials. The different ceramic materials are characterized by different sintering temperatures. A metal paste consisting of Pd, Ag, Ag-Pd, Ag-Pt, Cu and Ag is used to integrate electric components. A paste of the oxide CuO is also specified. The specification of the oxide would not lead a person skilled in the art to use structured metal foils instead of the metal pastes."

As noted by applicant, Nishikawa teaches forming the conductor circuits from a number of different materials such that clearly Nishikawa is not limited to any material and in particular copper oxide such that the argument that "The specification of the oxide would not lead a person skilled in the art to use structured metal foils instead of the metal pastes." is not persuasive.

Applicant further argues, "Sato is concerned ***exclusively*** with a body made of a ceramic and plastic composite. To produce the body, a single-layer, ceramic blank is sintered into a single-layer, porous ceramic body, which is subsequently impregnated with plastic. Following the production of the body made of the composite, metal foils made of copper are applied. Therefore, a joint sintering of the metal foils and a ceramic blank does not take place. This is also not possible because the plastic must be introduced into the pores of the ceramic body after sintering. As a result, a person skilled in the art, beginning with Nishikawa, would not consider the prior art according to Sato."

It is noted Sato is applied merely as evidence of the well known technique of forming electrodes (conductor circuits) from a number of functionally equivalent techniques including conductive paste and metal foils in assembling structures of the type taught by Nishikawa. Sato teaches, "When conductor circuits are formed on the electronic circuit substrate according to the invention, ***there may be employed various process usually used in the formation of printed wiring boards or hybrid IC boards***. For instance, there are a plating process, ***a process of adhering a metal foil, a process of using a resin conductor paste***, an evaporation process, ***a process of using a thick-film conductor paste***, a multi-wire process and a combination thereof." (See Column 5, lines 21-29 Emphasis added). Thus, clearly Sato teaches that the processes usually used in forming conductor circuits in products such ceramic circuit boards included conductive paste and metal foils. It is additionally noted, that there is nothing in Sato which suggests that applying a conductor circuit in the form of a metal foil to a green layer is only possible after the sheet is sintered.

Applicant further argues, "Lin relates to a ceramic multilayer substrate made of a glass ceramic material. The ceramic green foils used for this purpose are designed in such a way that the sintering temperature is as low as possible. The ceramic multilayer body is produced at a temperature of 850 ^{O}C to 950 ^{O}C in a one-step sintering process. This means that, in contrast to the claimed invention, a multistage sintering process is not provided. The multilayer substrate known from Lin is used, for example, as a carrier body for a silicone chip. For this reason, the thermal expansion coefficient of the substrate is adjusted to conform to the thermal expansion coefficients of silicone. A relatively broad range of between 3 and 8 ppm per ^{O}C is claimed for this purpose in Lin. However, because the entire ceramic multilayer body consists of one and the same ceramic material, it is not necessary to adjust the thermal expansion coefficients of individual layers in the multilayer body to one another. Thus, the goal and solution in Lin differs significantly from the goal and solution of the claimed invention. As a result, one of ordinary skill in the art would not be motivated to combine the teachings of Lin with the other cited references to arrive at the claimed invention."

It is noted Lin et al. is cited merely as evidence of it being known to use ceramic green layers having thermal coefficients of expansion below 8 ppm/K such that the coefficients of

expansion of the green layers essentially match those of the additional layers within the multilayer, e.g. electrodes, metal foils, conductive paste, etc., thus preventing the additional layers from cracking or distorting. There is nothing in Lin et al. to suggest that using thermal coefficients of expansion below 8 ppm/K would not be as applicable to a multistage sintering process as it would be to a single stage sintering process.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John L. Goff
May 6, 2004

JEFF H. AFTERGUT
PRIMARY EXAMINER
GROUP 1300